IBM Field Engineering Handbook

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System/360 Model 50

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System/360 Model 50

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Address comments concerning the contents of this publication to: IBM Corporation, FE Manuals, Dept. B96, PO Box 390, Poughkeepsie, New York 12602

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MACHINE VOLTAGES PRESENT WITH POWER OFF OR WITH DC OFF

1. 208 vac	In the power control compartment On the contactor gate At the CE panel circuit breakers At the convenience outlet transformer
2. 115 vac	At the convenience outlet transformer At relays 49, 50, 51, and 52
3. 48 vdc	On the relay gate On the contactor gate On the CE panel On the 48v bus On all thermals On all power supply terminal board positions 7, 8, and 9
4. 24 vac	In the power control compartments On the relay gate On the contactor gate At the console emergency off switch

LIST OF MODEL 50 MANUALS

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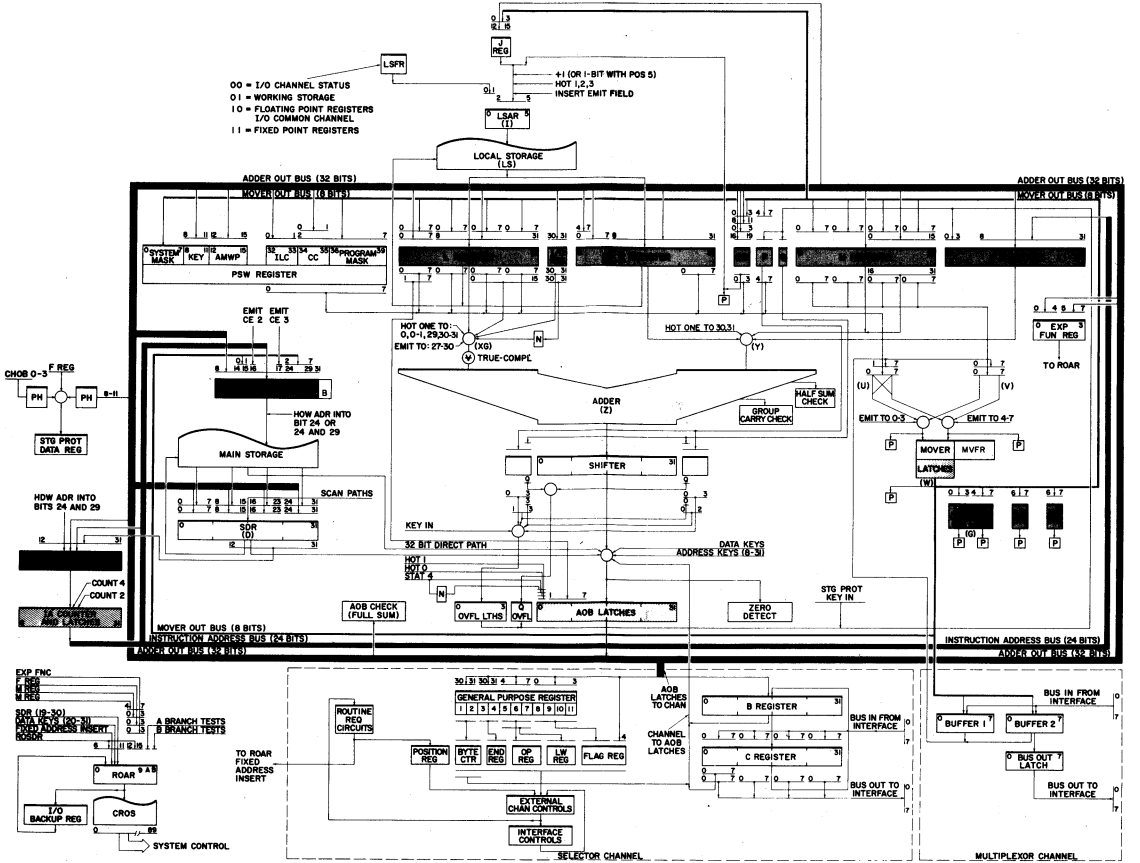
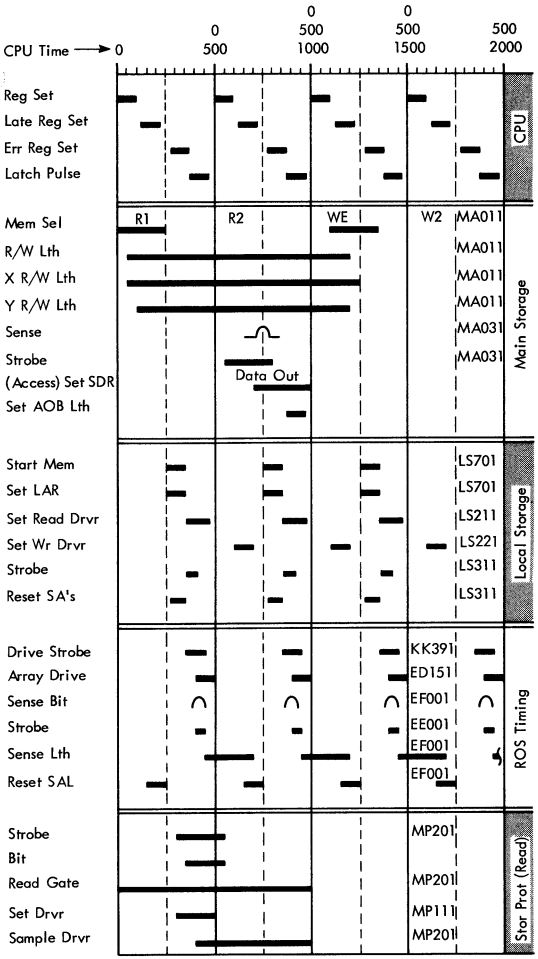
SYSTEM/360 MODEL 50 DATA FLOW

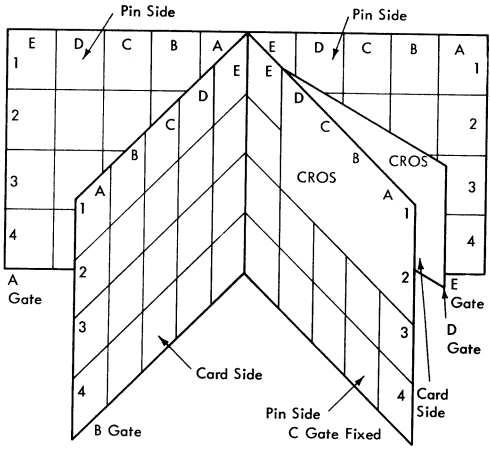


ALD PAGE INDEX

Edge Char	Format	Sym	Fld	Name	CE Page
E	0000 [binary]		CE	Control Emit Data	106
A	[RRR] ± [LLL] → [TTT]	R	RY	Right Input to Adder Y	107
		+	TC*	True - Complement Control	107
		[	LX	Left Input to Adder [XG]	107
		T	TR	Adder Latch Destination	102
	[UUUU] or [V→VVV→V]	U	AD*	Adder Function	107
		V	AL	Shift Gate and Adder Latch Control	104
B	[GGG] → U	G	LU	Mover Input, Left Side [U]	101
	[BBB] → V	B	MV	Mover Input, Right Side [V]	101
	[CCC] → WL [DDD] → WR	C	UL*	Mover Action 0-3	106
		D	UR*	Mover Action 4-7	106
	W → [FFF] or W [FF] → [FFF]	F	WM	Mover Output Destination	105
	SEMT		RY	(or SDR Parity Bits to CE Bits)	107
D	[AAAA] → [TTTT]	A	AL	Shift Control and Adder Latch In Gate	104
		T	TR	Adder Latch Destination	102
	[x] → LB, MB, MD or	X	UP*	Counter Function Control	105
	LB, MB, MD ± [x]	LB	LB	Select L Byte Counter	105
		MB	MB	Select M Byte Counter	105
		MD	MD	Select MD Counter	105
	[JJJJ] → ADDER or G [J] -1	J	DG	Length Ctr and Carry Insert Ctrl	105
L	[WWW] → LSA	W	WS*	Local Storage Addressing	103
	[SSS] → LS or LS → [SSS]	S	SF*	Local Storage Function	103
S	IA+ [Z] → A or IA+ [Z] → A, IA	Z	IV	Insn Address Reg Control	103
	HA → A		TR	Adder Latch Destination	102
	SMIF		ZN	(Suppress Memory Insn Fetch)	101
C	[Z/Z] → IVD IA + [Z] or IA + [Z/Z]	Z	IV	Invalid Digit Test	103
	All Others		SS	Stat Setting and Misc Control	111
R	[MMM] → ROAR or SCAN	M	ZF	Function Branch Control	101
	[P] Ω\ [P=P] → A or B	P	ZN*	ROS Address Control	101
	All others on R line		AB	ondition Test (Left ide)	98


0
0
0
0
500
500
500
CPU Time → 0
500
1000
1500
2000
Reg Set
Late Reg Set
Err Reg Set
Latch Pulse
CPU
Mem Sel
R/W Lth
X R/W Lth
Y R/W Lth
Sense
Strobe
(Access) Set SDR
Set AOB Lth
R1
R2
WE
W2
Data Out
MA011
MA011
MA011
MA011
MA031
MA031
Main Storage
Start Mem
Set LAR
Set Read Drvr
Set Wr Drvr
Strobe
Reset SA's
LS701
LS701
LS211
LS221
LS311
LS311
Local Storage
Drive Strobe
Array Drive
Sense Bit
Strobe
Sense Lth
Reset SAL
KK391
ED151
EF001
EE001
EF001
EF001
ROS Timing
Strobe
Bit
Read Gate
Set Drvr
Sample Drvr
MP201
MP201
MP111
MP201
Stor Prot (Read)

BOARD LOCATIONS IN GATES



ERROR REGISTER

Bit	Error Indicated
0	Half-Sum 0-7
1	Half-Sum 8-15
2	Half-Sum 16-23
3	Half-Sum 24-31
4	Sum 0-7
5	Sum 8-15
6	Sum 16-23
7	Sum 24-31
8	Carry
9	L Byte Counter
10	M Byte Counter
11	MD Counter
12	Length Counter (G1)
13	Length Counter (G2)
14	Mover Left Input
15	Mover Right Input
16	Mover Output
17	Storage Address Register 8-15
18	Storage Address Register 16-23
19	Storage Address Register 24-31
20	ROS 1-30
21	ROS 32-55
22	ROS 57-89
23	SP Check
24	LCS Check
25	Spare
26	Log Request

BOARD LAYOUT (SHEET 1 OF 2)

HINGE

GT-A

	A	B	C	D	E
1	A & B Branch Control	SAR-IAR Chan to Adr Lth	LTH & SDR 0-15 H Reg 0-15	G1 & G2 F & Q Reg 5 ROSDR Bits Gate Into L & H Control	12 ROSDR Bits Valid Digit Test Direct Cntl Mover Cntl
2	A & B Branch & Adder Test	Adder 0-15 Half Sum Chk 0-15	LTH & SDR 17-31 H Reg 16-31	MD Ctr W Parity W Checking	ROS Decode VFL Sign VFL Invalid Mover Br
3	Stats	Adder 16-31 Half Sum Chk 16-31	Gt Into Reg Cntl Adr Lth to Chan Full Sum Chk M Reg	Mover & Lth Mpx Bfr in Bus Term Mover Left & Right Gts	BAL & BAM WFCN LS Cntl LS Adr Chk Mover Edit J Reg
4	Stat & Feature Control	Emit Field X & Y Gating	LS S9 L Reg R Reg	S9 Local Store	S9 LSAR LSFN

GT-C

	A	B	C	D	E
1	CROS Gate-D Has Only a Top Portion and It is Part of CROS				CROS Logic
2					CROS Logic
3	CE Panel Mixing Board	ROAR Backup	CROS Control	CROS Control	CROS Control
4	CE Panel Mixing Board		Chan To Chan Adapter	1052 Adapter	1052 Adapter

HINGE

GT-B	A	B	C	D	E
1	Mpx Chan	Mpx Chan	Common Chan	MS Ripple Test Storage & Timing Holdoff	Inst Ctr Supervisory Cntls
2	Mpx Chan	Mpx Chan	Common Chan	Supervisory Cntls	Supervisory Cntls
3	Selector Chan 1	Selector Chan 1	Hi Speed Adapter	Selector Chan 1	Central Clock
4	Selector Chan 1	Selector Chan 1	Selector Chan 1	Selector Chan 1	

GT-E	A	B	C	D	E
1	Sel Chan 3	Sel Chan 3		Sel Chan 3	
2	Sel Chan 3	Sel Chan 3	Sel Chan 3	Sel Chan 3	
3	Sel Chan 2	Sel Chan 2	Common Chan	Sel Chan 2	
4	Sel Chan 2	Sel Chan 2	Sel Chan 2	Sel Chan 2	

1	I/O INSTRUCTION				CHAN NUMBER			INSTRUCTION REPLY						PRCD ON IRPT	TIME OUT	TIME OUT CHK	FOUL	
	START I/O	TEST I/O	HALT I/O	TEST CHAN	4	2	1	0	1	2	3	REPLY	BCHI					
2	RTNE RECD	PCI ENABL	BREAK IN	I/O RTNE	EARLY FIRST CYCLE	FIRST CYCLE	CHAIN FIRST CYCLE	LS RD	LS WR	CHAL DTC	ALCH DTC	CHAIN	LAST CYCLE	BREAK OUT	SBCR			
															0	1	2	3
3	BUFFER 1				BUFFER 2				BUFFER 3				I/O STATS					
	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	4	
4	BUFFER 1								BUFFER 2									
	P	0	1	2	3	4	5	6	7	P	0	1	2	3	4	5	6	7
5	SEL OUT	SEL IN	OP IN	SUP OUT	REQ IN	OUT			IN					BUS OUT				
						SVC	ADR	CMND	SVC	ADR	STAT			P	0	1	2	3
6	CONTROLLED EMIT				ROUTINE REQUEST TGRS				PRIORITY				CONTROL TRIGGERS						
	0	1	2	3	A	E1	E2	E3	E4	2	3	PCI	CC	DTC	UCW	IB FULL	POLL	BURST MODE
7																		
8																		

																		1
	ROS BITS				FIRST CYCLE CHK													2
	33	34	47	48														
I/O CHK MODE	LOGS																	3
	1	2	3	GATE STATUS	RESET													
					REQ LOG OUT													4
BUS OUT				CHECKS														5
4	5	6	7	PGRM	STOR PROT													
MPX I/O STATS				DATA XFER CNTL	CC RESET CNTL													6
0	1	2	3															
																		7
																		8

CONSOLE

1	B REGISTER																
	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
2	C REGISTER																	C
	P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
3	BYTE COUNTER						END REG		LAST WORDS			END OF RECORD						REGS
	A			B								COUNT			READ	B	LS	
	P	2	1	P	2	1	2	1	3	2	1	INTLK	1	2	INTLK	AC	ENABL	LS
4	POSITION REGISTER									CYCLE COUNTER PHASE A STEP				CLOCK			LS	PCI
	UA FETCH	CCW1 TYPE	CCW2 TYPE	UNIT SEL	RD STORE	WR FETCH	END UP	COMP	IRPT	0	1	2	3	A0	A1	STEP	REQ	REQ
5	POS REG TRF	INH RD STOR	A CLOCK				SP		INSN SCAN	CHAN IN USE	POLL	POLL IRPT END	INSN INH	BC RDY	UA TO BUS = 0	U SEL ADR OUT	COMPARE	
			A	B	C	D	D1	D2									=	≠
6		GENERAL PURPOSE REGISTER										FLAG REG						
		1	2	3	4	5	6	7				CDA	CC	SILI	SKIP	PCI	FIN	FIRST WORD
7																		
8																		

B REGISTER																	
P 16–23	16	17	18	19	20	21	22	23	P 24–31	24	25	26	27	28	29	30	31

C REGISTER																	
P 16–23	16	17	18	19	20	21	22	23	P 24–31	24	25	26	27	28	29	30	31

FULL		READ				WRITE			CHANNEL CHECKS								
B	C	BKWD	OP	RDY	IF	OP	RDY	IF	CD = PC TYPE	SIM	ILI	PRGM	STOR PROT	CHAN DATA	CHAN CTRL	IF CTRL	CHAIN 1

REQUEST REGISTER													COMMON CHAN DETECT				
PRIORITY									STAT					PRI	PRI		INH
1	2	3	0	1	2	3	4	5	0	1	2	3	LS	1	2-3	PCI	RTNE

												OUT			IN			
STOP	IF CDA FIRST BYTE	CD	BC MOD ENABL	WR CHAIN RDY	REC END	OP IN TEST	CHAN STOP	SEL OUT	STOP RTNE	SEL IN	OP IN	SVC	ADR	CMND	SVC	ADR	STAT

										MP								
	FIRST BYTE	TOTAL REC FETCH	WR CHAIN PRCD	STOP REL				STAT NEXT		C1	C2	C3	C4	SUP OUT	REQ IN	SVC OUT HOLD	BLOCK STAT IN

FLT Op Decoder

17(F)	1	L REGISTER																
		P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
23(F)	2	R REGISTER																
		P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
22(F)	3	M REGISTER																
		P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
21(F)	4	H REGISTER																
		P 0-7	0	1	2	3	4	5	6	7	P 8-15	8	9	10	11	12	13	14	15
	5	SAR																
		P 8-15	8	9	10	11	12	13	14	15	P 16-23	16	17	18	19	20	21	22	23
	6	ROS	CE				LX			TC	RY			AD					
		P 57-89	57	58	59	60	61	62	63	64	65	66	67	68	CL 69	70	71	72	73
	7	PRIORITY TRIGGERS			INSERT	REMOTE	STOR	STOR		LCS READY									
		REQ	MASTER	LAST CYCLE	PREFIX TGR	STOR READY	SYNC TGR	RING INH	INVAL ADDR	1	2	3	4						
	8	CHECK				UNIT IDENTITY													
		MARK	KEY	ADDR	DATE	1	2	3	4										

FLT Op Decoder

	L REGISTER																		1
17(F)	P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31	
	R REGISTER																		2
23(F)	P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31	
	M REGISTER																		3
22(F)	P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31	
	H REGISTER																		4
21(F)	P 16-23	16	17	18	19	20	21	22	23	P 24-31	24	25	26	27	28	29	30	31	
	SAR										BYTE STATS				BYTE STORE STATS				5
	P 24-31	24	25	26	27	28	29	30	31		0	1	2	3	0	1	2	3	
	AB				BB						SS								6
	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89			
																			7
																			8

FLT Op Decoder

1	ROS P 1-30	LU			MV		ZP							ZF				ZN	
		1	2	3	4	5	6	7	8	9	10	11		12	13	14	15	16	17
2	ROS P 32-55	IV CT			AL					WM WL				HC	UP MS		MD	LB CG	MB
		32	33	34	35	36	37	38	39	40	41	42		43	44	45	46	47	48
3	ONE SYL OP	RE-FETCH					NEXT ROS ADDRESS												
							ROS BASE ADDRESS							FUNCTION BIT				BRANCH	
							0	1	2	3	4	5		0	1	2	3	A	B
20	4	I/O MODE	I/O REGISTER			TIMER IRPT	CONS IRPT	L BYTE CNTR			M BYTE CNTR			F REG					Q REQ
			P	0	1			P	0	1	P	0	1	P	0	1	2	3	
24	5	LSAR						FN	LS		J REG					MD			
		P	0	1	2	3	4	5	0	1	P	0	1	2	3	P	0	1	2
12	6	ADDER									COUNTERS					MOVER			LSAR
		HALF SUM				SUM										INPUTS		OUT-PUT	
		0-7	8-15	16-23	24-31	0-7	8-15	16-23	24-31	CARRY	L BYTE	M BYTE	MD	G1	G2	L	R		
	7							CURRENT ROS ADDRESS											
								0	1	2	3	4	5	6	7	8	9	10	11
	8							PREVIOUS ROS ADDRESS											
								0	1	2	3	4	5	6	7	8	9	10	11

FL, Op Decoder

ZN		TR						WS			SF								
								CS	SA										
18		19	20	21	22	23	24	25	26	27	28	29	30						1
DG		UL		UR			MOVER FUNCTION												
MG							CPU			I/O									
49	50	51	52	53	54	55	0	1	2	0	1	2							2
EXTERNAL INTERRUPT REGISTER						PSW													
						ILC		CC		PM									
1	2	3	4	5	6	32	33	34	35	36	37	38	39						3
EDIT STATS		GENERAL PURPOSE STATS												STORAGE RING					
										L	R								
20 1	2	0	1	2	3	4	5	6	7	SIGN	SIGN	CARRY	RTL	R1	R2	R3	W1		4
MD		G1						G2											
24 3		S	P	0	1	2	3	S	P	0	1	2	3						5
SAR			ROS																
12						PROT		LOG											
8-15	16-23	24-31	1-30	32-55	57-89	TAG	LCS	REQ											6
																			7
																			8

Common/Multiplexor Channel Status													
Word 1		Word 2		Word 3		Word 4		Word 5		Word 6	
START I/O	KE001	RTNE RCVD	KE301		0	KE341		P	FA011	SEL OUT	FA141		0	FA063
TEST I/O	KE001	PCI ENABL	KE131	BUFFER	1	KE341		0	FA011	SEL IN	FA361	CONTROLLED	1	FA063
HALT I/O	KE001	BREAK IN	KE301	1	2	KE351		1	FA011	OP IN	FA361	EMIT	2	FA063
TEST CHAN	KE001	I/O RTNE	KE311		3	KE351	BUFFER	2	FA021	SUP IN	FA151		3	FA063
4	KE021	EARLY FIRST CYC	KE301		0	KE341	1	3	FA021	REQ IN	FA361		A	FA171
CHAN 2	KE021	FIRST CYC	KE301	BUFFER	1	KE341		4	FA021	SVC OUT	FA141	RTNE	E1	FA171
1	KE021	CHAIN FIRST CYC	KE321	2	2	KE351		5	FA031	ADR OUT	FA131	REQ	E2	FA171
NUMBER 0	KE051	LS RD	KE471		3	KE351		6	FA031	CMND OUT	FA141	TGRS	E3	FA171
INSTR 1	KE051	LS WR	KE471		0	KE341		7	FA031	SVC IN	FA351		E4	FA171
REPLY 2	KE061	CHAL DTC	KE441	BUFFER	1	KE341		P	FA011	ADR IN	FA351		2	FA261
3	KE061	ALCH DTC	KE441	3	2	KE351		0	FA011	STAT IN	FA351	PRIORITY	3	FA261
REPLY	KE071	CHAIN	KE321		3	KE351		1	FA011		FA051		PCI	FA261
BCHI	KE141	LAST CYC	KE321		0	KE151	BUFFER	2	FA021	P	FA051		CC	FA251
PRCD ON IRPT	KE101	BREAK OUT	KE321		1	KE161	2	3	FA021	0	FA051		DTC	FA261
TIME OUT	KE091			I/O	2	KE171		4	FA021	1	FA051	CTRL	UCW	FA251
TIME OUT CHK	KE091	SBCR 0	KE381	STATS	3	KE181		5	FA031	BUS 2	FA051		IB FULL	FA331
FOUL	KE091	1	KE381		4	KE191		6	FA031	OUT 3	FA051		POLL	FA341
IOHS	KE191	2	KE381	I/O CHK MODE		KE311		7	FA031	4	FA051		BURST MODE	FA311
		3	KE381			KE661	REQ LOG OUT		FA341	5	FA051	MPX	0	FA091
		33	KE441		1	KE661				6	FA051	I/O	1	FA101
		ROS 34	KE441	LOGS	2	KE661				7	FA051	STATS	2	FA111
		BITS 47	KE321		3	KE661				PRGM CHK	FA371		3	FA121
		48	KE321	GATE STATUS		KE671				STOR PROT CHK	FA371			
		FIRST CYC CHK	KE531	RESET		KE671						DATA XFR CTRL		FA071
												CC RESET CTRL		FA252

Selector Channel Status																							
Word 1			Word 2			Word 3			Word 4			Word 5			Word 6								
B REG			C REG																				
P0-7		GH101	P0-7		GH101	BYTE	P	GR131	UA FETCH		GB181	POS REG TRF		GB171			1	GC101
0		GH111	0		GH111	CTR	2	GR131	CCW1 TYPE		GB181	INH RD STOR		GG131			2	GC101
1		GH121	1		GH121	A	1	GR131	CCW2 TYPE		GB181		A	GA101	GENERAL		3	GC101
2		GH131	2		GH131	BYTE	P	GR131	UNIT SEL		GB181	A	B	GA101	PURPOSE		4	GC101
3		GH141	3		GH141	CTR	2	GR131	RD STORE		GB181	CLOCK	C	GA101	REG		5	GC121
4		GH151	4		GH151	B	1	GR131	WR FETCH		GB181		D	GA101			6	GC121
5		GH161	5		GH161	END	2	GC111	END UP		GB181	SP	D1	GA161			7	GC121
6		GH171	6		GH171	REG	1	GC111	COMPARE		GB181		D2	GA161			CDA	GC161
7		GH181	7		GH181	LAST	3	GC141	INTERRUPT		GB181	INSN SCAN		GF111	FLAG		CC	GC161
P8-15		GJ101	P8-15		GJ101	WORDS	2	GC141	CYCLE	0	GA131	CHAN IN USE		GF111	REG		SILI	GC161
8		GJ111	8		GJ111		1	GC141	CTR	1	GA131	POLL		GR121			SKIP	GC161
9		GJ121	9		GJ121		CNT INTLK	GC151	PHASE A	2	GA131	POLL IRPT END		GR121			PCI	GC161
10		GJ131	10		GJ131	EOR	1	GC151	STEP	3	GA131	INSN INH		GD131	FINISH			GB161
11		GJ141	11		GJ141		2	GC151		A0	GA111	BC RDY		GF141	FIRST WORD			GF161
12		GJ151	12		GJ151		RD INTLK	GC151	CLOCK	A1	GA111	UA TO BUS = 0		GV121	FIRST BYTE			GF161
13		GJ161	13		GJ161		BAC	GG131		STEP	GA111	UNIT SEL ADR OUT		GV121	TOTAL REC FETCH			GF111
14		GJ171	14		GJ171	LS ENABL		GG131	LS REQ		GG101	COMPARE	=	GR151	WR CHAIN PRCD			GT131
15		GJ181	15		GJ181		LS	GC171	PCI REQ		GG181		≠	GR151	STOP REL			GV111
P16-23		GK101	P16-23		GK101	REG	B	GC171			GB141	STOP		GV101	STAT NEXT			GT161
16		GK111	16		GK111	FULL	C	GT141	PRIORITY	1	GB141	IF CDA FIRST BYTE		GT161			C1	GA141
17		GK121	17		GK121		BKWD	GC131		2	GB151	CD		GF111	MP		C2	GA141
18		GK131	18		GK131	READ	OP	GC131		3	GB101	BC MOD ENABL		GR141			C3	GA151
19		GK141	19		GK141		RDY	GF161		0	GB101	WR CHAIN RDY		GF161			C4	GA151
20		GK151	20		GK151		IF	GT121	REQUEST	1	GB101	REC END		GF111	SUP OUT			GS131
21		GK161	21		GK161		OP	GC131	REG	2	GB101	OP IN TEST		GR101	REQ IN			GS141
22		GK171	22		GK171	WRITE	RDY	GF161		3	GB111	CHAN STOP		GE121	SVC OUT HOLD			GV151
23		GK181	23		GK181		IF	GT121		4	GB111	SEL OUT		GR101	BLOCK STAT IN			GS111
P24-31		GL101	P24-31		GL101		CD=PC TYPE	GE111		5	GB131	STOP RTNE		GV101				
24		GL111	24		GL111		SIM	GG131	STATS	0	GB121	SEL IN		GS121				
25		GL121	25		GL121		ILI	GE111		1	GB121	OP IN		GS121				
26		GL131	26		GL131	CHAN	PGRM	GE111		2	GB121	SVC OUT		GS131				
27		GL141	27		GL141	CHKS	STOR PROT	GE111		3	GB131	ADR OUT		GS131				
28		GL151	28		GL151		CHAN DATA	GE111		LS	GA030	CMND OUT		GS131				
29		GL161	29		GL161		CHAN CTRL	GE101	COM	PRI 1	GA030	SVC IN		GS111				
30		GL171	30		GL171		IF CTRL	GE101	CHAN	PRI 2-3	GA030	ADR IN		GS111				
31		GL181	31		GL181		CHAIN 1	GE111	DETECT	PCI	GA030	STAT IN		GS111				
										INH RTNE	GA030							

CPU #1 Status																							
Word 1				Word 2				Word 3				Word 4				Word 5				Word 6			
L REG				R REG				M REG				H REG				SAR							
P0-7	RL001			P0-7	RR001			P0-7	RM001			P0-7	RH001			P8-15	RA061			ROS	P57-89		RK301
0	RL001			0	RR001			0	RM001			0	RH001			8	RA003				57		RK301
1	RL001			1	RR001			1	RM001			1	RH001			9	RA003				58		RK301
2	RL001			2	RR001			2	RM001			2	RH001			10	RA002			CE	59		RK301
3	RL001			3	RR001			3	RM001			3	RH001			11	RA002				60		RK301
4	RL011			4	RR011			4	RM011			4	RH011			12	RA002				61		RK311
5	RL011			5	RR011			5	RM011			5	RH011			13	RA002			LX	62		RK311
6	RL011			6	RR011			6	RM011			6	RH011			14	RA001				63		RK311
7	RL011			7	RR011			7	RM011			7	RH011			15	RA011			TC	64		RK311
P8-15	RL021			P8-15	RR021			P8-15	RM021			P8-15	RH021			P16-23	RA061				65		RK311
8	RL021			8	RR021			8	RM021			8	RH021			16	RA011			RY	66		RK311
9	RL021			9	RR021			9	RM021			9	RH021			17	RA011				67		RK311
10	RL021			10	RR021			10	RM021			10	RH021			18	RA011				68		BH061
11	RL021			11	RR021			11	RM021			11	RH021			19	RA011			CL	69		BH061
12	RL031			12	RR031			12	RM031			12	RH031			20	RA021			AD	70		BH061
13	RL031			13	RR031			13	RM031			13	RH031			21	RA021				71		BH061
14	RL031			14	RR031			14	RM031			14	RH031			22	RA021				72		RK331
15	RL031			15	RR031			15	RM031			15	RH031			23	RA021				73		RK331
P16-23	RL041			P16-23	RR041			P16-23	RM041			P16-23	RH041			P24-31	RA061			AB	74		RK331
16	RL041			16	RR041			16	RM041			16	RH041			24	RA021				75		RK331
17	RL041			17	RR041			17	RM041			17	RH041			25	RA031				76		RK331
18	RL041			18	RR041			18	RM041			18	RH041			26	RA031				77		RK331
19	RL041			19	RR041			19	RM041			19	RH041			27	RA031				78		RK341
20	RL051			20	RR051			20	RM051			20	RH051			28	RA031				79		RK341
21	RL051			21	RR051			21	RM051			21	RH051			29	RA031			BB	80		RK341
22	RL051			22	RR051			22	RM051			22	RH051			30	RA061				81		RK341
23	RL051			23	RR051			23	RM051			23	RH051			31	RA061				82		RK341
P24-31	RL061			P24-31	RR061			P24-31	RM061			P24-31	RH061			0	KS001				84		RK351
24	RL061			24	RR061			24	RM061			24	RH061			BYTE 1	KS001				85		RK351
25	RL061			25	RR061			25	RM061			25	RH061			STATS 2	KS001			SS	86		RK351
26	RL061			26	RR061			26	RM061			26	RH061			3	KS011				87		RK351
27	RL061			27	RR061			27	RM061			27	RH061			BYTE 0	KS021				88		RK351
28	RL071			28	RR071			28	RM071			28	RH071			STORE 1	KS021				89		RK351
29	RL071			29	RR071			29	RM071			29	RH071			STATS 2	KS031						
30	RL071			30	RR071			30	RM071			30	RH071			3	KS031						
31	RL071			31	RR071			31	RM071			31	RH071										

CPU #2 Status

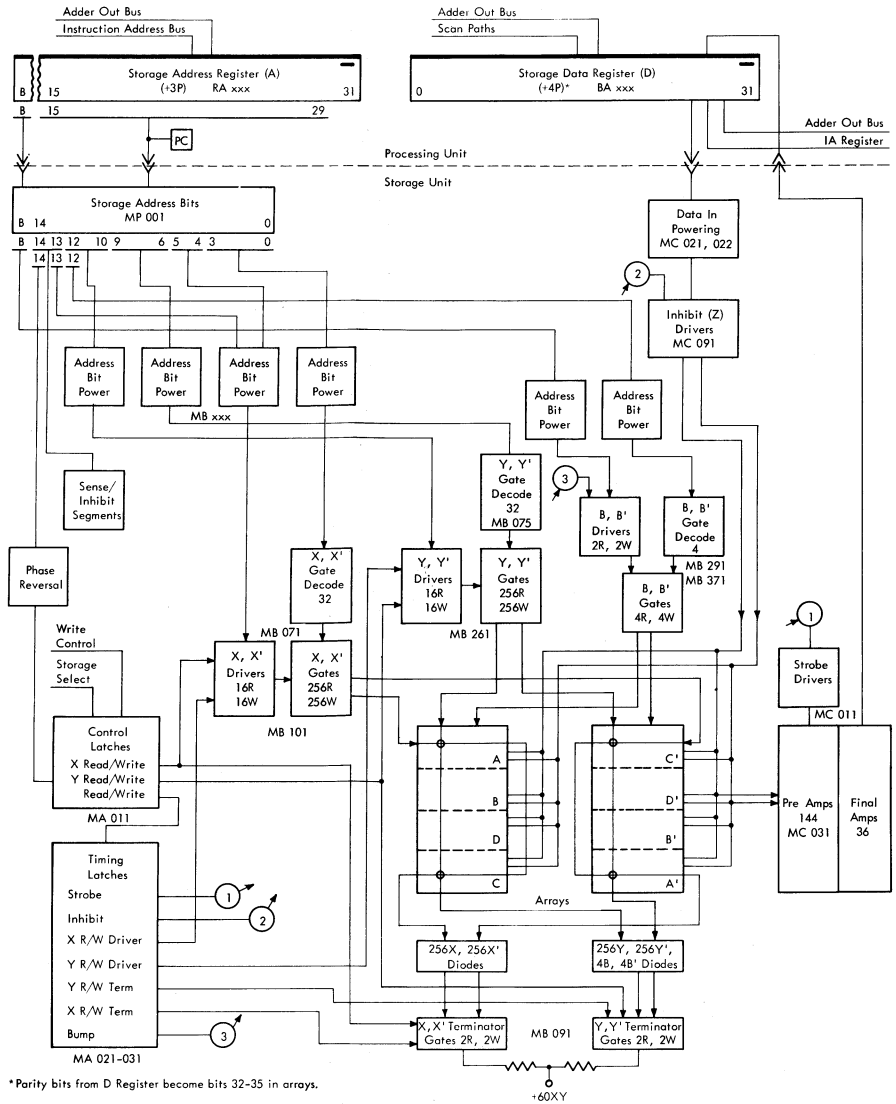
Word 1			Word 2			Word 3			Word 4			Word 5			Word 6		
ROS	P1-30	BH091	ROS	P30-55	RK211	ONE SYL OP		KS221	I/O MODE		KU111		0	LS111		0-7	KT011
	1	RK121		32	RK201	RE-FETCH		KS211	I/O	P	RL111		1	LS111		8-15	KT011
LU	2	RK121	IV-CT	33	RK201		0	KK301	REG	0	RL111		2	LS111	HALF	16-23	KT011
	3	RK121		34	RK201	ROS	1	KK301		1	RL111	LSAR	3	LS121	SUM	24-31	KT011
	4	RK121		35	RK211	BASE	2	KK311	TIMER IRPT		KS251		4	LS121		0-7	KT011
MV	5	RK121		36	RK211	ADR	3	KK311	CONS IRPT		KS251		5	LS121		8-15	KT011
	6	KK301	AL	37	RK211		4	KK321		P	CL001		0	KL001	SUM	16-23	KT011
	7	KK301		38	RK211		5	KK301	L BYTE	0	CL001	LSFN	1	KL001		24-31	KT011
ZP	8	KK311		39	RK211	NEXT	0	KK011	CNTR	1	CL001		P	RJ011	CARRY		KT021
	9	KK311		40	RK221	ROS	FUNCT 1	KK021		P	CM001	J	0	RJ001		L BYTE	KT021
	10	KK321	WL	41	RK221	ADDR	BIT 2	KK031	MB	0	CM001	REG	1	RJ001	CNTRS	M BYTE	KT021
	11	KK301	WM	42	RK221		3	KK041	CNTR	1	CM001		2	RJ001		MD	KT021
	12	KK001	HC	43	RK221		A	KK261		P	RF021		3	RJ001		G1	KT031
ZF	13	KK001	UP	44	RK221		BRANCH B	KK271	F	0	RF001		P	CD021		G2	KT031
	14	KK001	MS	45	RK221		1	KS271	REG	1	RF001	MD	0	CD001	MVR IN L		KT021
	15	KK001	MD	46	RK231	EXT	2	KS271		2	RF001	CTR	1	CD001	MVR IN R		KT021
	16	KK003	LB	47	RK231	IRPT	3	KS271		3	RF011		2	CD011	MVR OUT		KT021
ZN	17	KK003	CG MB	48	RK231	REG	4	KS281	Q REG		RF031		3	CD011		8-15	KT031
	18	KK003		49	RK231		5	KS281	EDIT	1	KK581		S	KP031	SAR	16-23	KT031
	19	RK101	DG-MG	50	RK231		6	KS281	STATS	2	KK581		P	CG101		24-31	KT031
	20	RK101		51	RK231	ILC	32	RP001		0	KS101	G1	0	CG101		1-30	KT031
TR	21	RK101	UL	52	RK201		33	RP001		1	KS111		1	CG101	ROS	32-55	KT031
	22	RK101		53	RK201	CC	34	RP011		2	KS121		2	CG101		57-89	KT031
	23	RK101	UR	54	RK201		35	RP021	GP	3	KS131		3	CG101	PROT TAG		KT041
CS-	25	RK111		55	RK201	PSW	36	RP001	STATS	4	KS141		S	KP031	LCS		
WS SA	26	RK111	MVR	0	KQ001		37	RP001		5	KS151		P	CG201	LOG REQ		KT041
	27	RK111	FUNCT	1	KQ001	PM	38	RP001		6	KS161		0	CG201			
SF	28	RK111	CPU	2	KQ001		39	RP001		7	KS171	G2	1	CG201			
	29	RK111	MVR	0	KQ001				L SIGN		KS201		2	CG201			
	30	RK111	FUNCT	1	KQ001				R SIGN		KS201		3	CG201			
			I/O	2	KQ001				CARRY		KS231						
									RTL		KS631						
										R1	KC501						
									STORAGE	R2	KC501						
									RING	R3	KC501						
										W1	KC501						

CPU #2 Status			
Word 7		Word 8	
CURRENT ROS ADDRESS		PREVIOUS ROS ADDRESS	
0	KK312	0	KK312
1	KK312	1	KK312
2	KK312	2	KK312
3	KK312	3	KK312
4	KK312	4	KK312
5	KK312	5	KK312
6	KK313	6	KK313
7	KK313	7	KK313
8	KK313	8	KK313
9	KK313	9	KK313
10	KK313	10	KK313
11	KK313	11	KK313

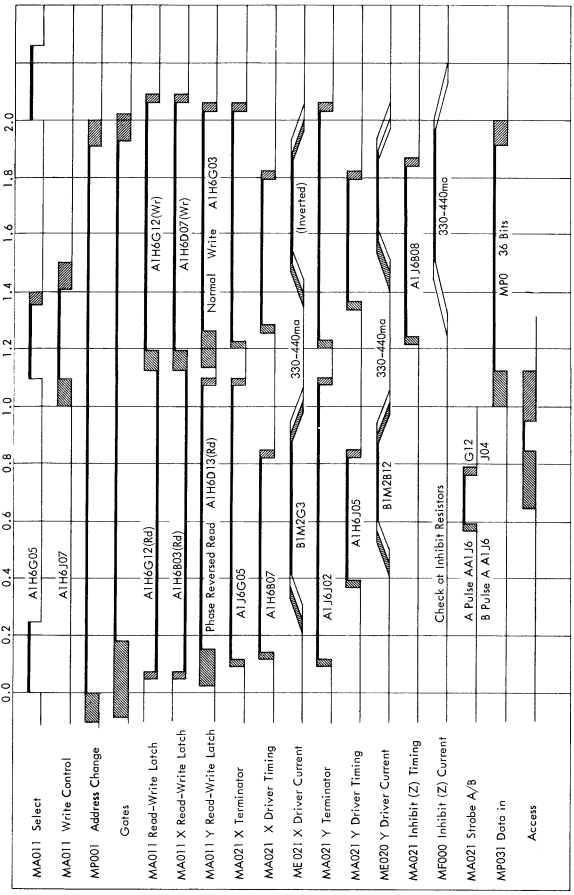
INDICATOR LATCH LOCATION TABLE (SHEET 5 OF 5)

SDR		IAR		Maintenance Chk	
P0-7	BA072	P8-15	CA171	PASS	KH321
0	BA001	8	CA161	FAIL	KH321
1	BA011	9	CA161	BINARY TGR	KH211
2	BA021	10	CA161	TEST CTR = 0	KH311
3	BA031	11	CA161	0	KH111
4	BA041	12	CA151	FLT 1	KH111
5	BA051	13	CA151	OP 2	KH111
6	BA061	14	CA151	REG 3	KH111
7	BA071	15	CA151	4	KH111
P8-15	BA152	P16-23	CA171	5	KH111
8	BA081	16	CA141	SEQ 4	KH341
9	BA091	17	CA141	CTR 2	KH341
10	BA101	18	CA141	1	KH341
11	BA111	19	CA141	1	KH345
12	BA121	20	CA131	SEQ 2	KH345
13	BA131	21	CA131	STAT 3	KH345
14	BA141	22	CA131	4	KH345
15	BA151	23	CA131	FLT LD CHK	KH555
P16-23	BA232	P24-31	CA171	SUPV STAT	KH321
16	BA161	24	CA121	PROGSV SCAN STAT	KH321
17	BA171	25	CA121	SUPV ENABL STOR	KH321
18	BA181	26	CA121	SEQ CTR	KT151
19	BA191	27	CA121	MODE MAIN STOR	KT151
20	BA201	28	CA111	ROS	KT151
21	BA211	29	CA111	ALT PREFIX	
22	BA221	30	CA111	HARD STOP	KT161
23	BA231	31	CA111	LOG TGR	KT151
P24-31	BA312			BLOCK IND	KH231
24	BA241	System Status		SINGLE CYC	KT271
25	BA251			CPU	KT215
26	BA261			CLOCK CHAN	KT211
27	BA271	MASTER CHK	KT081	ROS	KT211
28	BA281	LOAD	PL031	MAIN STOR	KT211
29	BA291	TEST	PK101	IRPT CHK ENABLD	KT161
30	BA301	WAIT	PK101	CHK REG GATED	KT161
31	BA311	MANUAL	PK101	CHK PEND	KT081
		SYSTEM	PK101		

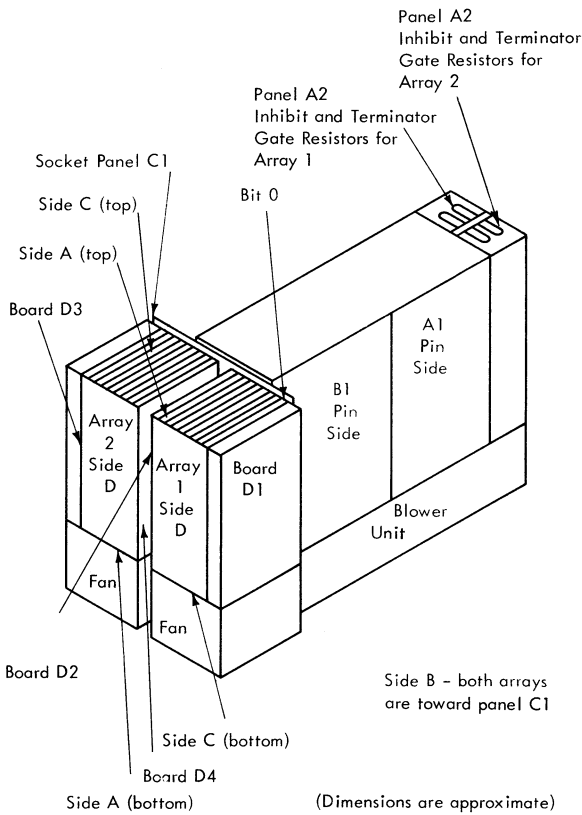
CODE	MEANING
0 00000	No Op
1 00001	ROSDR Gr #1 to Bus (0-30)
2 00010	ROSDR Gr #2 to Bus (31-55)
3 00011	ROSDR Gr #3 to Bus (56-87)
4 00100	ROSDR Gr #4 to Bus (88-89)
5 00101	ROAR to Bus
6 00110	Request for ROS Control
7 00111	SDR to ROAR and Reset Binary Trigger
8 01000	Reset Error Register
9 01001	No Op
10 01010	Request FLT Load
11 01011	Inhibit SAR Gating - Stop
12 01100	Error Register to Bus
13 01101	No Op
14 01110	SDR to IAR IFF Binary Trigger Equals Zero
15 01111	Step Binary Trigger if SDR is All Ones
16 10000	SAR to Bus
17 10001	L Register to Bus
18 10010	Sel Chan to Bus
19 10011	Sel Chan Parity to Bus
20 10100	Stats to Bus
21 10101	H Register to Bus
22 10110	M Register to Bus
23 10111	R Register to Bus
24 11000	LSAR to Bus
25 11001	Mpx Chan Gr #1 to Bus
26 11010	Mpx Chan Gr #2 to Bus
27 11011	Mpx Chan Gr #3 to Bus
28 11100	Common Chan Gr #1 to Bus
29 11101	Common Chan Gr #2 to Bus
30 11110	Common Chan Gr #3 to Bus
31 11111	No Op



*Parity bits from D Register become bits 32-35 in arrays.


0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
MA011 Select
A1H6G05
MA011 Write Control
A1H6J07
MP001 Address Change
Gates
MA011 Read-Write Latch
A1H6G12(Rd)
A1H6G12(Wr)
MA011 X Read-Write Latch
A1H6803(Rd)
A1H6D07(Wr)
MA011 Y Read-Write Latch
Phase Reversed Read
A1H6D13(Rd)
Normal Write
A1H6G03
MA021 X Terminator
A1J6G05
MA021 X Driver Timing
A1H6807
ME021 X Driver Current
B1M2G3
330–440ma
(Inverted)
MA021 Y Terminator
A1J6J02
MA021 Y Driver Timing
A1H6J05
ME020 Y Driver Current
B1M2B12
330–440ma
MA021 Inhibit (Z) Timing
A1J6808
MF000 Inhibit (Z) Current
Check at Inhibit Resistors
330–440ma
MA021 Strobe A/B
A Pulse AA1J6
G12
B Pulse A A1J6
J04
MP031 Data in
MP0
36 Bits
Access

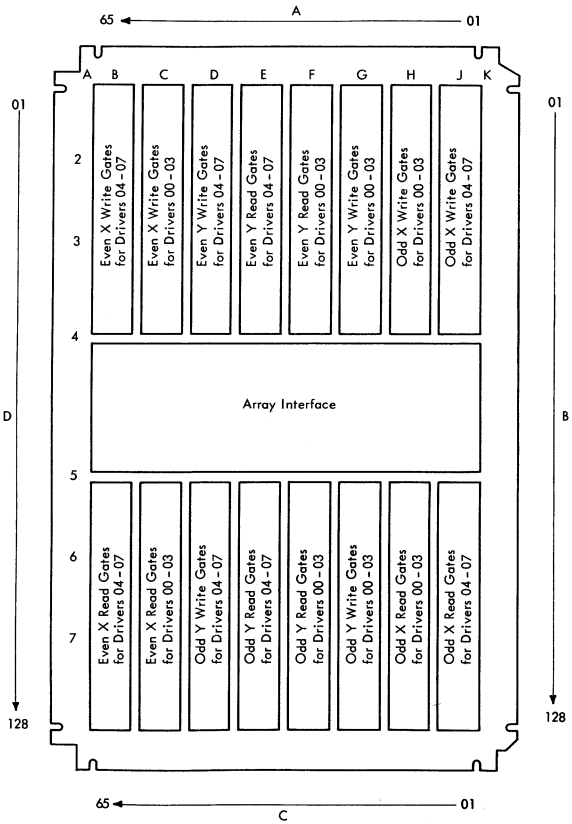
ARRANGEMENT OF UNITS OF STORAGE



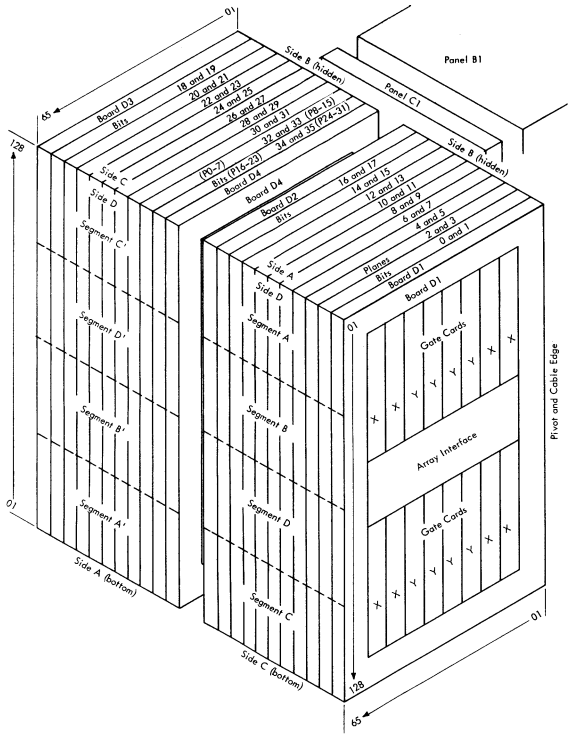
MAIN STORAGE CABLE COLOR CODING

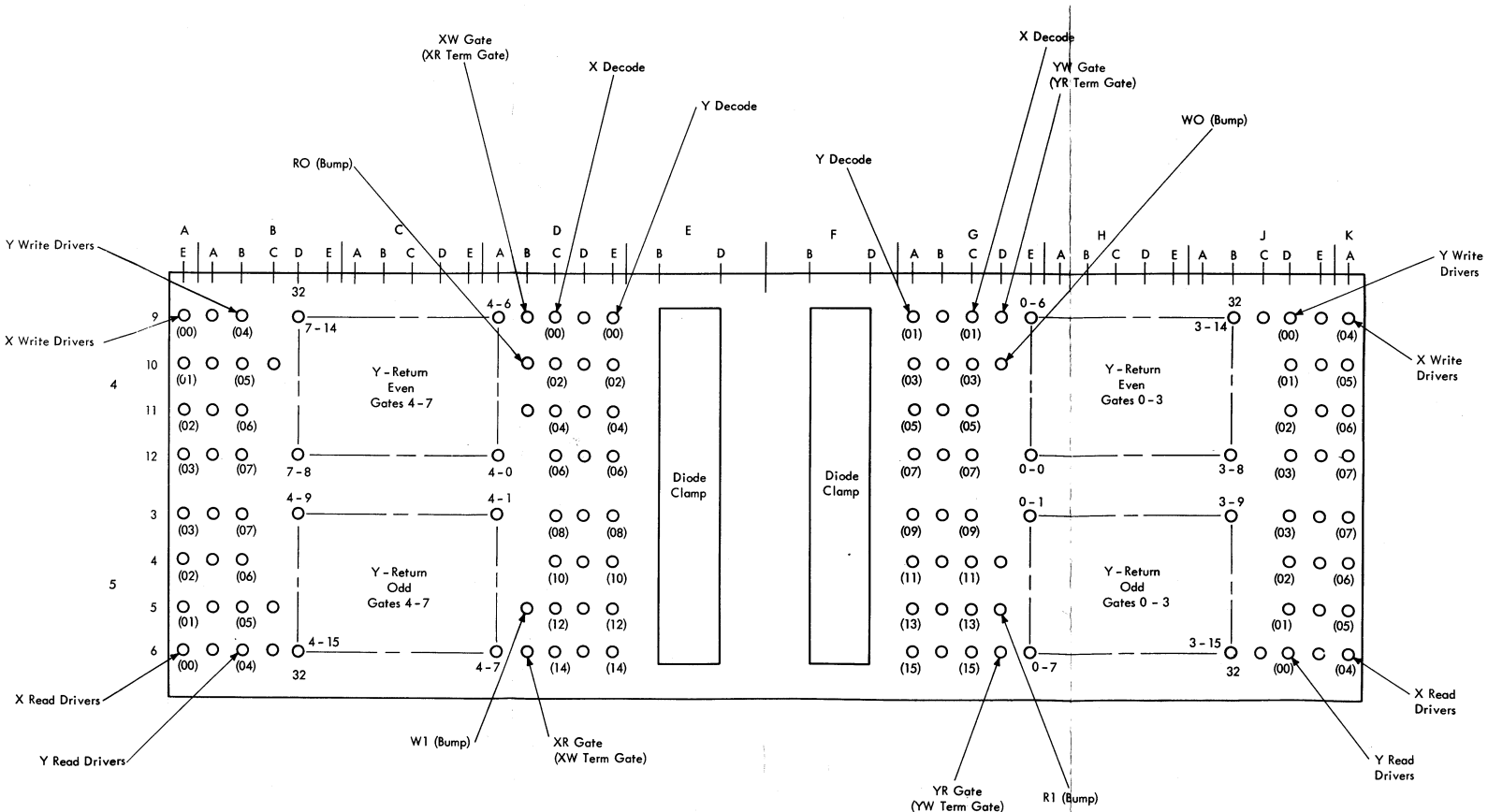
Blue
White
Black
} Sense-Inhibit Lines

Gray - 4 wires to terminator gates per array.
Black and Brown - gate decode lines.
Black and Orange - read-write drivers.
Purple - bump circuits.


A
65
01
A
B
C
D
E
F
G
H
J
K
01
01
D
B
2
3
4
5
6
7
Even X Write Gates for Drivers 04-07
Even X Write Gates for Drivers 00-03
Even Y Write Gates for Drivers 04-07
Even Y Read Gates for Drivers 04-07
Even Y Read Gates for Drivers 00-03
Even Y Write Gates for Drivers 00-03
Odd X Write Gates for Drivers 00-03
Odd X Write Gates for Drivers 04-07
Array Interface
Even X Read Gates for Drivers 04-07
Even X Read Gates for Drivers 00-03
Odd Y Write Gates for Drivers 04-07
Odd Y Read Gates for Drivers 04-07
Odd Y Read Gates for Drivers 00-03
Odd Y Write Gates for Drivers 00-03
Odd X Read Gates for Drivers 00-03
Odd X Read Gates for Drivers 04-07
128
128
65
01
C

STORAGE ARRAY END BOARD D1




XW Gate
(XR Term Gate)
X Decode
Y Decode
RO (Bump)
X Decode
YW Gate
(YR Term Gate)
WO (Bump)
Y Decode
Y Write Drivers
X Write Drivers
Y Write Drivers
X Write Drivers
Y - Return
Even
Gates 4 - 7
Y - Return
Odd
Gates 4 - 7
Y - Return
Even
Gates 0 - 3
Y - Return
Odd
Gates 0 - 3
Diode
Clamp
Diode
Clamp
X Read Drivers
Y Read Drivers
W1 (Bump)
XR Gate
(XW Term Gate)
YR Gate
(YW Term Gate)
R1 (Bump)
X Read
Drivers
Y Read
Drivers

Main Storage

Storage Address Register		10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Address Bits	B						14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Decode Function							ø Rev	X Dvr	Y Drivers			Y Gates				X Drivers		X Gates					
Decode Value								4	4	2	1	8	4	2	1	2	1	8	4	2	1		
Other Bit Functions							Seg Select															Byte	

Bump Storage

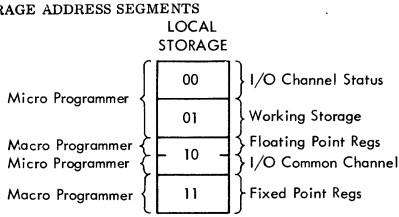
Input Source	WS or Mask Order		W (1)	Emit			W					
				2	3		2	3	4	5	6	7
Bump Decode Functions	B Bit		ø Rev	X Dvrs	B Gate		X Drivers		X Gates			
Decode Value	1			4	1		2	1	8	4	2	1

NOTE: W (0) is used to determine which BOM is addressed.

ADDRESS BITS 13 AND 14 RELATIONSHIP TO STROBE--INHIBIT SEGMENTS, PLANES AND ADDRESSES

Address Bit 14	Address Bit 13	Strobe Pulse	Strobe Bytes	Strobe Segments	Inhibit Segments	Planes (Bits) Array 1	Planes (Bits) Array 2	Addresses
		B	0,2	A, A'	A, A'	0 - 8	18 - 26	0000-8191
	1	B	0,2	B, B'	B, B'	0 - 8	18 - 26	8192-16383
1		A	0,2	C, C'	C, C'	0 - 8	18 - 26	16384-24575
1	1	A	0,2	D, D'	D, D'	0 - 8	18 - 26	24576-32767
		A	1,3	A, A'	A, A'	9 - 17	27 - 35	0000-8191
	1	A	1,3	B, B'	B, B'	9 - 17	27 - 35	8192-16383
1		B	1,3	C, C'	C, C'	9 - 17	27 - 35	16384-24575
1	1	B	1,3	D, D'	D, D'	9 - 17	27 - 35	24576-32767

LOCAL STORAGE ADDRESS SEGMENTS



I/O CHANNEL STATUS

Sector Word Selector Channel One
- 00 0000 Command Address
- 0001 Data Address
- 0010 Word Count
- 0011 Data Buffer

Selector Channel Two
- 00 0100 Command Address
- 0101 Data Address
- 0110 Word Count
- 0111 Data Buffer

Selector Channel Three
- 00 1000 Command Address
- 1001 Data Address
- 1010 Word Count
- 1011 Data Buffer

Multiplex Channel
- 00 1100 Command Address
- 1101 Data Address
- 1110 Word Count
- 1111 Unit Address

WORKING STORAGE

Sector Word Entire sector is micro-programmer scratchpad.
- 01 Word 0111 is PSW left half backup. Word 1110 is the Operation Buffer.

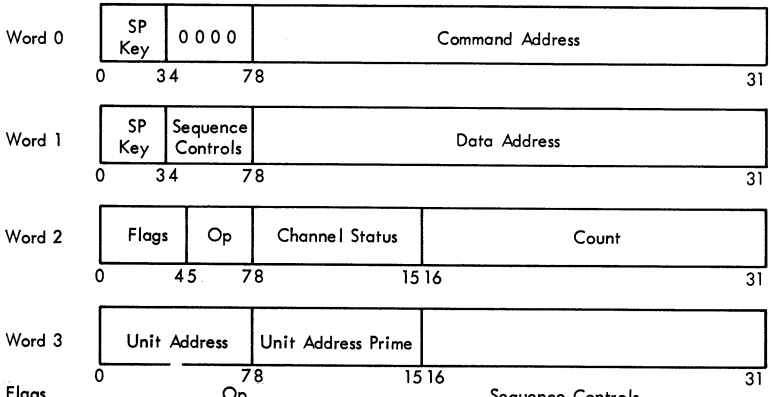
10 FLOATING POINT REGISTERS

Words 0000 thru 0111 are FP registers 1-4 (double word registers).

10 I/O COMMON CHANNEL
- 1000 Not used
- 1001 Not used
- 1010 Not used
- 1011 Not used
- 1100 R Reg Break-In Buffer
- 1101 Mpx Channel L Reg Buffer
- 1110 Mpx Channel Interrupt Buffer
- 1111 Mpx Channel Working Storage

11 GENERAL REGISTER

Entire sector is macro-programmer scratchpad



Flags

0 CD
1 CC
2 SILI
3 Skip
4 PCI

Op

000 - Input Forward
001 - Input Backward
110 - Output Forward
011 - Input Skip
111 - Stop
100 - End Status AND Not WLR
101 - End Status AND WLR

Sequence Controls

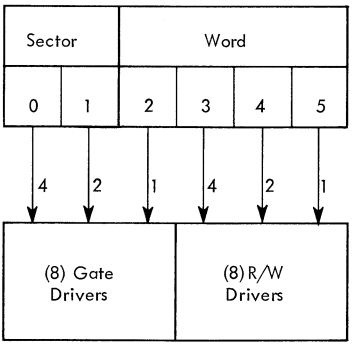
0000 - Idle
0001 - Busy
0011 - CC End Read
0101 - Chan End in 1B
0111 - Chan End Qued
0110 - Device End/Attention in 1B

Channel Status

0 PCI
1 WLR
2 Program Check
3 Protection Check
4 Channel Data Check
5 Channel Control Check
6 Interface Control Check
7 Chaining Check

LOCAL STORAGE

BUMP STORAGE



GATE DRIVERS

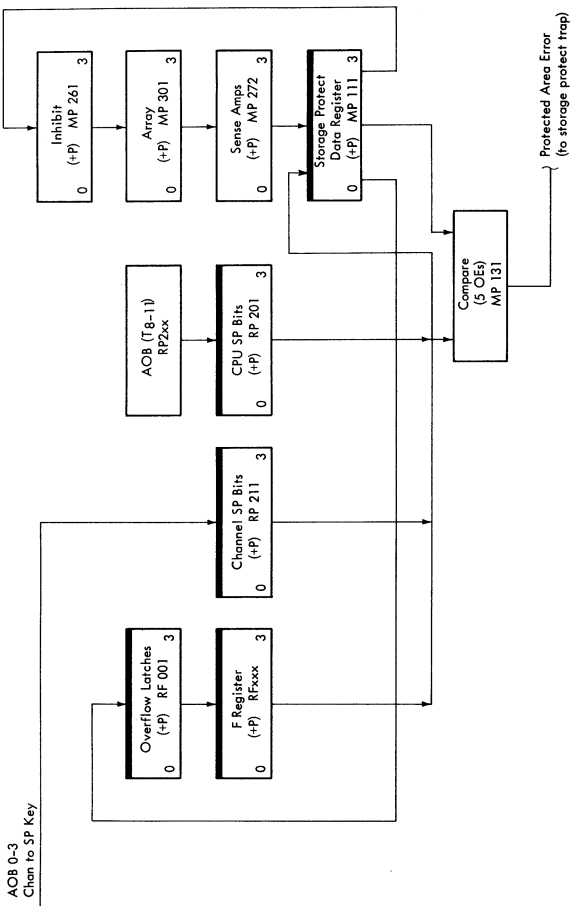
	0	1	2	3	4	5	6	7
7	7	15	23	31	39	47	55	63
6	6	14	22	30	38	46	54	62
5	5	13	21	29	37	45	53	61
4	4	12	20	28	36	44	52	60
3	3	11	19	27	35	43	51	59
2	2	10	18	26	34	42	50	58
1	1	9	17	25	33	41	49	57
0	0	8	16	24	32	40	48	56
	0		1		2		3	

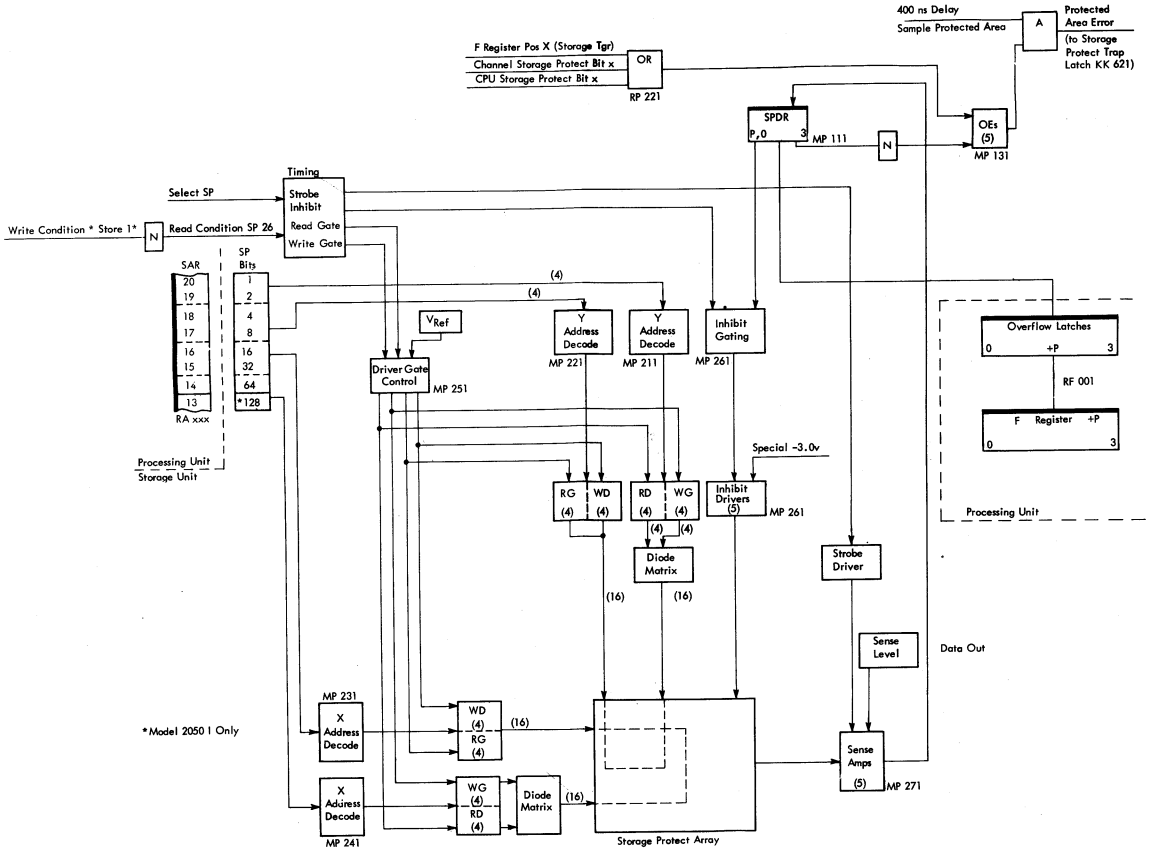
GATE DRIVERS

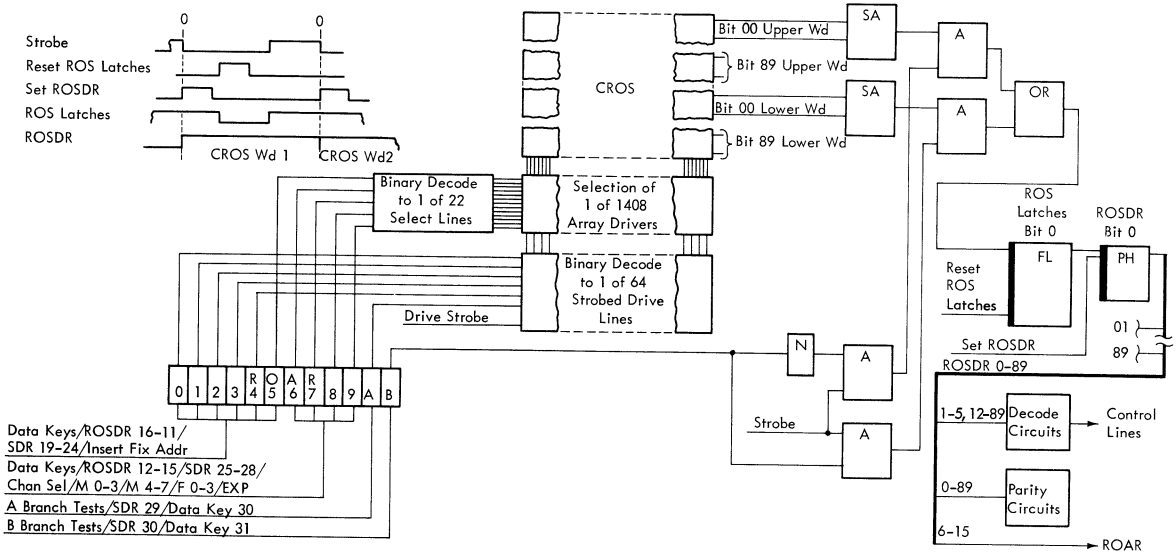
SECTOR

2050 Model	Bytes of Main Storage	Positions of SP	X Address					Y Address			
			SAR	13	14	15	16	17	18	19	20
F	65K	32					16	8	4	2	1
G	131K	64	SP			32	16	8	4	2	1
H	262K	128	Bits		64	32	16	8	4	2	1
I	524K	256		128	64	32	16	8	4	2	1

STORAGE PROTECT


Inhibit (+P) MP 261 0 3
Array (+P) MP 301 0 3
Sense Amps (+P) MP 272 0 3
Storage Protect Data Register (+P) MP 111 0 3
AOB (T 8-11) RP2xx
CPU SP Bits (+P) RP 201 0 3
Compare (5 OEs) MP 131
Protected Area Error (to storage protect trap)
Channel SP Bits (+P) RP 211 0 3
Overflow Latches (+P) RF 001 0 3
F Register (+P) RFxxx 0 3
AOB 0-3 Chan to SP Key


400 ns Delay
Sample Protected Area
A
Protected Area Error
(to Storage Protect Trap Latch KK 621)
F Register Pos X (Storage Tgr)
Channel Storage Protect Bit x
CPU Storage Protect Bit x
OR
RP 221
SPDR
P,0 3
MP 111
N
OEs (5)
MP 131
Timing
Select SP
Strobe Inhibit
Read Gate
Write Gate
Write Condition * Store 1*
N
Read Condition SP 26
SAR
SP Bits
20 19 18 17 16 15 14 13
RA xxx
1 2 4 8 16 32 64 *128
(4)
(4)
VRef
Y Address Decode
MP 221
Y Address Decode
MP 211
Inhibit Gating
MP 261
Overflow Latches
0 +P 3
RF 001
F Register +P
0 3
Driver Gate Control
MP 251
Special -3.0v
Processing Unit
Storage Unit
RG (4)
WD (4)
RD (4)
WG (4)
Inhibit Drivers (5)
MP 261
(4) (4)
Diode Matrix
(16)
(16)
Strobe Driver
Processing Unit
Sense Level
Data Out
MP 231
X Address Decode
*Model 2050 I Only
WD (4)
RG (4)
(16)
WG (4)
RD (4)
Diode Matrix
(16)
Sense Amps (5)
MP 271
X Address Decode
MP 241
Storage Protect Array



READ-ONLY STORAGE

BINARY DECODE OF ROAR TO 1 OF 64 DRIVER LINES

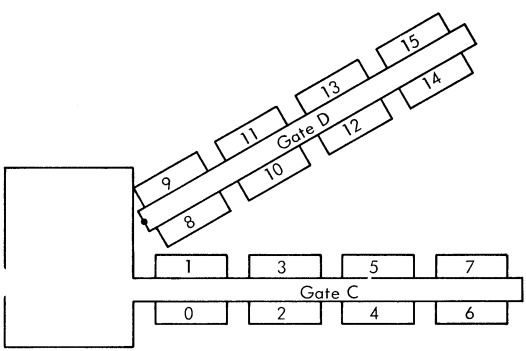
Base Addresses			First Drive Lines	Base Address		Second Drive Lines	Decoded Drive Lines	
BA0	BA1	BA2		BA3	BA4		No A Branch Bit	A Branch Bit
				0	0	SD0	Drive 0 P00-QP0	Drive 1 P00-QP1
0	0	0	FD0	0	1	SD1	Drive 2 P00-QP2	Drive 3 P00-QP3
				1	0	SD2	Drive 4 P01-QP0	Drive 5 P01-QP1
				1	1	SD3	Drive 6 P01-QP2	Drive 7 P01-QP3
				0	0	SD4	Drive 8 P02-QP0	Drive 9 P02-QP1
0	0	1	FD1	0	1	SD5	Drive 10 P02-QP2	Drive 11 P02-QP3
				1	0	SD6	Drive 12 P03-QP0	Drive 13 P03-QP1
				1	1	SD7	Drive 14 P03-QP2	Drive 15 P03-QP3
				0	0	SD8	Drive 16 P04-QP0	Drive 17 P04-QP1
0	1	0	FD2	0	1	SD9	Drive 18 P04-QP2	Drive 19 P04-QP3
				1	0	SD10	Drive 20 P05-QP0	Drive 21 P05-QP1
				1	1	SD11	Drive 22 P05-QP2	Drive 23 P05-QP3
				0	0	SD12	Drive 24 P06-QP0	Drive 25 P06-QP1
0	1	1	FD3	0	1	SD13	Drive 26 P06-QP2	Drive 27 P06-QP3
				1	0	SD14	Drive 28 P07-QP0	Drive 29 P07-QP1
				1	1	SD15	Drive 30 P07-QP2	Drive 31 P07-QP3
				0	0	SD16	Drive 32 P08-QP0	Drive 33 P08-QP1
1	0	0	FD4	0	1	SD17	Drive 34 P08-QP2	Drive 35 P08-QP3
				1	0	SD18	Drive 36 P09-QP0	Drive 37 P09-QP1
				1	1	SD19	Drive 38 P09-QP2	Drive 39 P09-QP3
				0	0	SD20	Drive 40 P10-QP0	Drive 41 P10-QP1
1	0	1	FD5	0	1	SD21	Drive 42 P10-QP2	Drive 43 P10-QP3
				1	0	SD22	Drive 44 P11-QP0	Drive 45 P11-QP1
				1	1	SD23	Drive 46 P11-QP2	Drive 47 P11-QP3
				0	0	SD24	Drive 48 P12-QP0	Drive 49 P12-QP1
1	1	0	FD6	0	1	SD25	Drive 50 P12-QP2	Drive 51 P12-QP3
				1	0	SD26	Drive 52 P13-QP0	Drive 53 P13-QP1
				1	1	SD27	Drive 54 P13-QP2	Drive 55 P13-QP3
				0	0	SD28	Drive 56 P14-QP0	Drive 57 P14-QP1
1	1	1	FD7	0	1	SD29	Drive 58 P14-QP2	Drive 59 P14-QP3
				1	0	SD30	Drive 60 P15-QP0	Drive 61 P15-QP1
				1	1	SD31	Drive 62 P15-QP2	Drive 63 P15-QP3

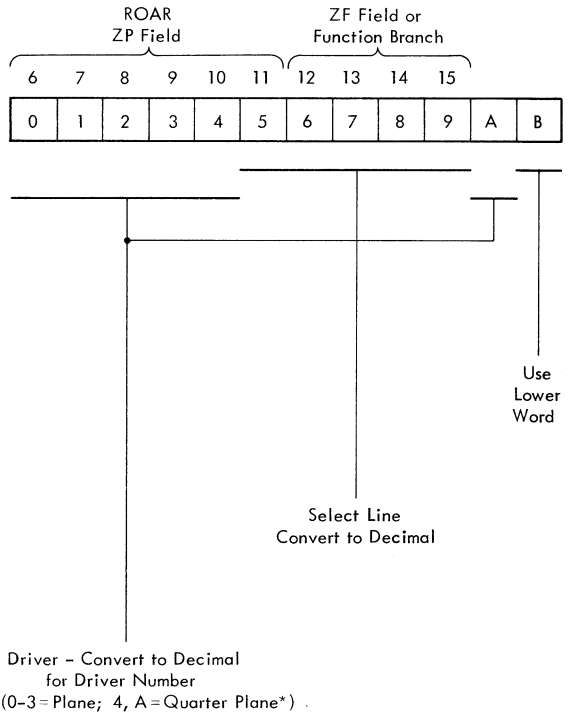
BINARY DECODE OF ROAR TO SELECT LINES

Select Lines	ROAR Positions				
	5	6	7	8	9
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	-	0	1	1	0
7	-	0	1	1	1
8	-	1	0	0	0
9	-	1	0	0	1
10	-	1	0	1	0
11	-	1	0	1	1
12	-	1	1	0	0
13	-	1	1	0	1
14	-	1	1	1	0
15	-	1	1	1	1
16	1	-	0	0	0
17	1	-	0	0	1
18	1	-	0	1	0
19	1	-	0	1	1
20	1	-	1	0	0
21	1	-	1	0	1

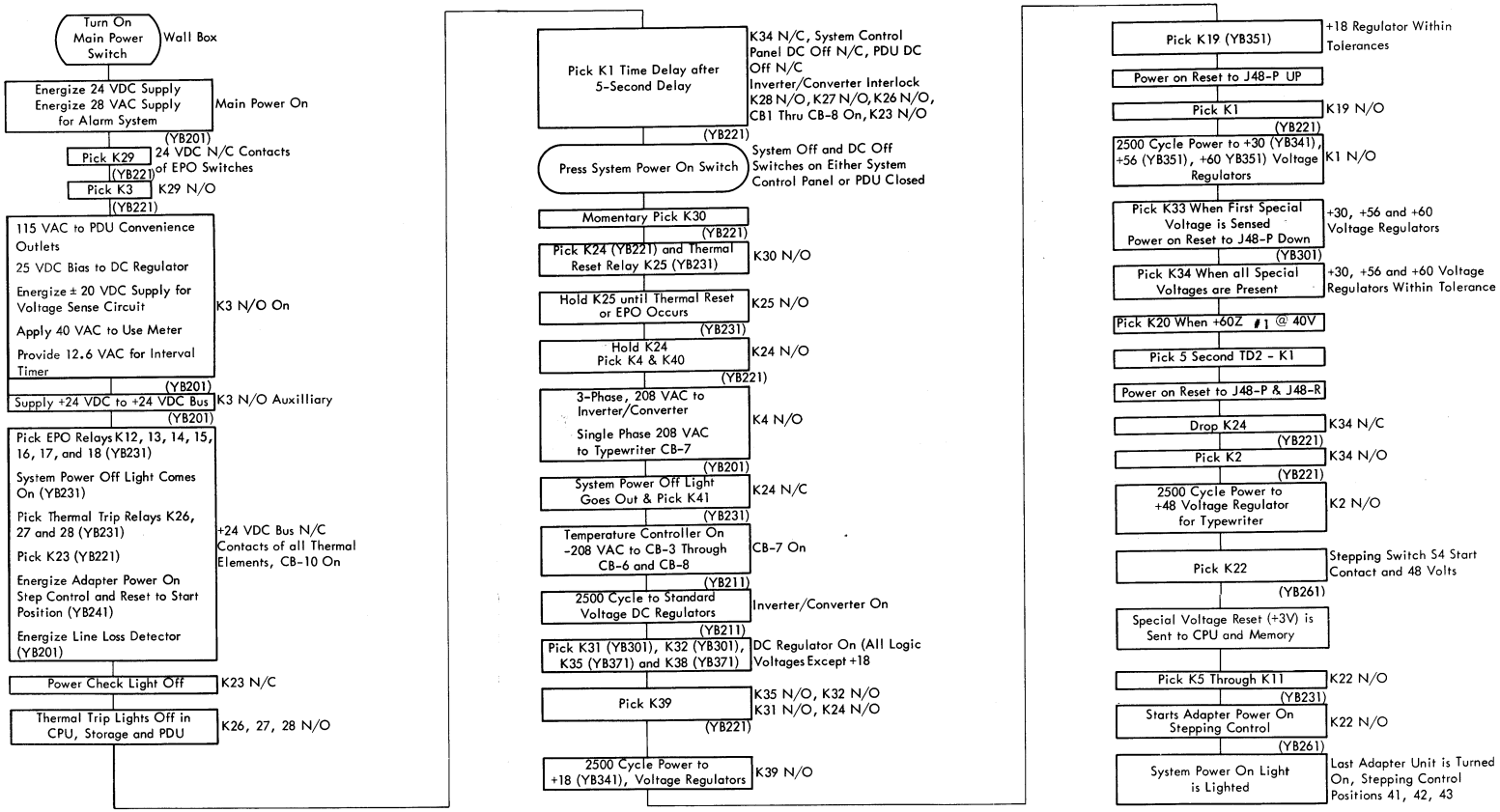
Select Lines 0-5 are decoded from ROAR Pos 5, 6, 7, 8, and 9
Select Lines 6-15 are decoded from ROAR Pos 6, 7, 8, and 9
Select Lines 16-21 are decoded from ROAR Pos 5, 7, 8, and 9

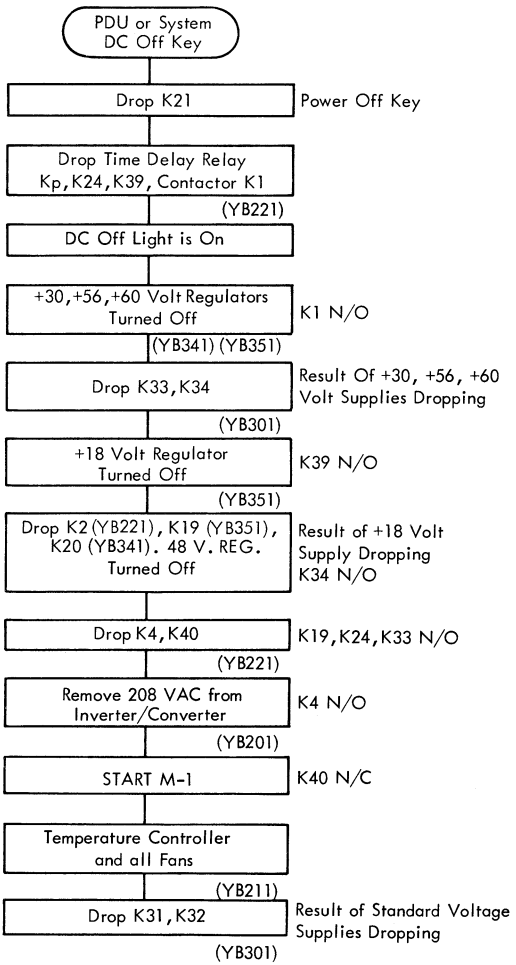
CROS PLANE LOCATIONS - TOP VIEW





*Quarter planes are numbered left to right from pressure plate side


Turn On Main Power Switch
Wall Box
Energize 24 VDC Supply
Energize 28 VAC Supply for Alarm System
Main Power On
(YB201)
Pick K29
24 VDC N/C Contacts of EPO Switches
(YB221)
Pick K3
K29 N/O
(YB221)
115 VAC to PDU Convenience Outlets
25 VDC Bias to DC Regulator
Energize ± 20 VDC Supply for Voltage Sense Circuit
Apply 40 VAC to Use Meter
Provide 12.6 VAC for Interval Timer
K3 N/O On
(YB201)
Supply +24 VDC to +24 VDC Bus
K3 N/O Auxilliary
(YB201)
Pick EPO Relays K12, 13, 14, 15, 16, 17, and 18 (YB231)
System Power Off Light Comes On (YB231)
Pick Thermal Trip Relays K26, 27 and 28 (YB231)
Pick K23 (YB221)
Energize Adapter Power On Step Control and Reset to Start Position (YB241)
Energize Line Loss Detector (YB201)
+24 VDC Bus N/C Contacts of all Thermal Elements, CB-10 On
Power Check Light Off
K23 N/C
Thermal Trip Lights Off in CPU, Storage and PDU
K26, 27, 28 N/O
Pick K1 Time Delay after 5-Second Delay
K34 N/C, System Control Panel DC Off N/C, PDU DC Off N/C
Inverter/Converter Interlock K28 N/O, K27 N/O, K26 N/O, CB1 Thru CB-8 On, K23 N/O
(YB221)
Press System Power On Switch
System Off and DC Off Switches on Either System Control Panel or PDU Closed
Momentary Pick K30
(YB221)
Pick K24 (YB221) and Thermal Reset Relay K25 (YB231)
K30 N/O
Hold K25 until Thermal Reset or EPO Occurs
K25 N/O
(YB231)
Hold K24
Pick K4 & K40
K24 N/O
(YB221)
3-Phase, 208 VAC to Inverter/Converter
Single Phase 208 VAC to Typewriter CB-7
K4 N/O
(YB201)
System Power Off Light Goes Out & Pick K41
K24 N/C
(YB231)
Temperature Controller On -208 VAC to CB-3 Through CB-6 and CB-8
CB-7 On
(YB211)
2500 Cycle to Standard Voltage DC Regulators
Inverter/Converter On
(YB211)
Pick K31 (YB301), K32 (YB301), K35 (YB371) and K38 (YB371)
DC Regulator On (All Logic Voltages Except +18
Pick K39
K35 N/O, K32 N/O
K31 N/O, K24 N/O
(YB221)
2500 Cycle Power to +18 (YB341), Voltage Regulators
K39 N/O
Pick K19 (YB351)
+18 Regulator Within Tolerances
Power on Reset to J48-P UP
Pick K1
K19 N/O
(YB221)
2500 Cycle Power to +30 (YB341), +56 (YB351), +60 YB351) Voltage Regulators
K1 N/O
Pick K33 When First Special Voltage is Sensed
Power on Reset to J48-P Down
+30, +56 and +60 Voltage Regulators
(YB301)
Pick K34 When all Special Voltages are Present
+30, +56 and +60 Voltage Regulators Within Tolerance
Pick K20 When +60Z #1 @ 40V
Pick 5 Second TD2 - K1
Power on Reset to J48-P & J48-R
Drop K24
K34 N/C
(YB221)
Pick K2
K34 N/O
(YB221)
2500 Cycle Power to +48 Voltage Regulator for Typewriter
K2 N/O
Pick K22
Stepping Switch S4 Start Contact and 48 Volts
(YB261)
Special Voltage Reset (+3V) is Sent to CPU and Memory
Pick K5 Through K11
K22 N/O
(YB231)
Starts Adapter Power On Stepping Control
K22 N/O
(YB261)
System Power On Light is Lighted
Last Adapter Unit is Turned On, Stepping Control Positions 41, 42, 43


PDU or System DC Off Key
Drop K21
Power Off Key
Drop Time Delay Relay Kp, K24, K39, Contactor K1
(YB221)
DC Off Light is On
+30, +56, +60 Volt Regulators Turned Off
K1 N/O
(YB341) (YB351)
Drop K33, K34
Result Of +30, +56, +60 Volt Supplies Dropping
(YB301)
+18 Volt Regulator Turned Off
K39 N/O
(YB351)
Drop K2 (YB221), K19 (YB351), K20 (YB341). 48 V. REG. Turned Off
Result of +18 Volt Supply Dropping K34 N/O
Drop K4, K40
K19, K24, K33 N/O
(YB221)
Remove 208 VAC from Inverter/Converter
K4 N/O
(YB201)
START M-1
K40 N/C
Temperature Controller and all Fans
(YB211)
Drop K31, K32
Result of Standard Voltage Supplies Dropping
(YB301)

SELECTOR CHANNEL LATCHES

Name	ALD Page
A Clock	GA101
A Clock Output	GA111
Address Compare	GR151
Address In	GS111
Address Req 0-3	GB171
B AC	GG131
B Clock	GA121
B Full	GC171
B Reg	GHxxx
B Reg Gate Ctl	GM101
BC	GR131
BC Decoding	GN191
BC = ER	GC111
BC Mod Req	GF141
BC Mod Enable	GR141
BC Ready	GF141
Bus In, Out	GNxxx
Byte Ctr	GR131
C Full	GT141
C Reg	GHxxx
C Reg Gate	GM111
C Reg Set	GM111
CC Step 0, 1, 2, 3	GA131
Checks, Channel	GE101
Checks From CPU	GD101
Clock A0, Al, Step	GA111
Clock B1, B2	GA121
Compare =, ≠	GR151
Condition Codes	GD141
Cycle Ctr	GA131
DTC	GD101
D1, D2	GA161
EOR Cnt Intlck	GC151
EOR 1, 2	GC151
ER 1, 2	GC111
Finish	GB161
First Byte	GF161
First Word	GF161
Flag Reg	GC161
GP BC Set A, B	GA121

Name	ALD Page
GP BC Xfer Gt	GC111
GP 1-4	GC101
GP 5-7	GC121
GP 8-11	GC161
Idle Mode	GF111
IF Bus In, Out	GN101
IF Poll	GR121
IF Out Tags	GS131
IF In Tags	GS111
IF Read	GT121
IF Service	GS111
IF Status	GS111
IF Stop	GV101
IF System Reset	GS151
IF Write	GT121
Inh Rd Store	GG131
Inst Inhibit	GD131
Instructions	GD131
Instruction Scan	GF111
ITD Logic	GR111
L1, 2, 3W	GC141
Log-Ind Bus	GPxxx
Log Wd Ctl	GD111
Log-Stop Req	GE121
LS DTC	GD101
LS Enable	GG131
LS Full	GC171
LS Req	GG101
MP C1, C2	GA141
MP C3, C4	GA151
Op In Test	GR101
Op Reg	GC131
Out Tags	GS131
Parity Checker IF	GT101
Parity Generator, Status	GE131
PCI Enable	GG181
PCI Req	GG181
Poll Int End	GR121
Poll Int Rej	GR121
Poll	GR121

SELECTOR CHANNEL LATCHES (Cont'd)

Name	ALD Page
Pos Reg	GB181
Pos Reg Xfer	GB171
Read Intlk	GC151
Read Op	GC131
Read Bkwd	GC131
Read LS Req	GC101
Read Rdy	GF161
Read Store Req	GG101
Record End	GF111
Reg Xfer (B to C)	GT141
Req Reg 0-3	GB101
Req Reg 4-5	GB111
Req Reg Pri 1, 2	GB141
Req Reg Pri 3	GB151
Req Reg Stat 0, 3, 4	GB131
Req Reg Stat 1, 2	GB121
Req Reg Xfer	GB171
Reset Ctls	GE191
Reset Req	GV111
Sel Out	GR101
Service In	GS111
Sim Ck	GG131
Stat B	GV111
Stat Next	GT161
Stat In	GS111
Stop	GV101
Stop Rel	GV111
Stop Rtne	GV101
Supp Out	GR101
SVC Out Hold	GV151
Tag Gate Generator	GR111
Time Out	GD131
Total Rec Fetch	GF111
UA to Bus 0	GV121
Unit Sel Addr Out	GV121
Unit Sel	GB181
WR Chain Proc	GT131
Wr Chain Rdy	GF161
Wr Fetch Req	GG141
Wr Op	GC131
Wr Ready	GF161

Signal	W 0-7 Bits on the mover-out bus	CPU stats 4-7 Identifies the signal after the stat 3 relay	Function
Interrupt Test I/O	1000 0000	1001	Issued to the multiplexor channel for a device end interrupt. The channel will set the unit status in M (0-7). The unit address is in L (0-7)
Time-out Check	0100 0000	X X X 0	Issued when the channel fails to respond (in 8 cycles) to the time-out signal with a stat 3 reply
Time-out	0010 0000	X X X 0	Issued when the "153 countdown loop" counts to zero without a stat 3 reply
Foul on Start I/O	0001 0000	0010	Issued when the CAW is invalid
Test Channel	0000 1000	0000	Requests the common channel circuits to test the state of the channel addressed by bits 21-23 of the L register, and set the condition code to identify the state of the channel
Test I/O	0000 0100	0100	Issued to initiate a channel routine to test the status of the I/O unit addressed by bits 21-31 of the L register. The channel either loads the R and M registers with CSW data, or sets the condition code
Halt I/O	0000 0100	0000	Issued to halt the data transfer occurring in the I/O unit addressed by bits 21-31 of the L register. The channel either loads the R and M registers with CSW data, or sets the condition code
Start I/O	0000 0001	0010	Issued to initiate the I/O command specified by the CCW-1 in the M register. The CAW is in the R register and the unit and channel address is in the L register

Common Channel Decode Lines	Emit Field	Function
CECC A-CC Emit 0	0000	Selector channel interrupt routine in process. Generates an immediate stat 3 reply
CECC A-CC Emit 1	0001	Log reset. Resets the selector channel after a selector channel log-out
CECC A-CC Emit 2	0010	Gate Status. Gates the selector channel status to the CPU after a log-out
CECC A-CC Emit 3	0011	Sets the interface register
CECC A-CC Emit 4	0100	Sets the scan channel latch
CECC A-CC Emit 5	0101	Sets the log trigger
CECC A-CC Emit 6	0110	Resets the common channel and multiplexor channel after log-out
CECC A-CC Emit 7	0111	Local store "Write DTC"
CECC B-CC Emit 1	1001	Proceed on Interrupt signal. Selector channel starts to load the L, R, and M registers with CSW data. Multiplexor channel generates an immediate stat 3 reply
CECC B-CC Emit 2	1010	Selector channel end update test
CECC B-CC Emit 3	1011	High speed channel time-out

REPLIES (Different Combinations are Decoded by the Status of CPU Stats 0, 1, 2, and 3)

Request	X001	X011	X101	X111	Countdown/No Reply
Foul on Start I/O	The start I/O would not have been excuted because the subchannel is busy or unavailable. Don't recognize the invalid CAW as a program check. The CC is set to 2 or 3 and the microprogram returns to I-fetch	not valid	The multiplexor channel requests a reset of the countdown. At the moment, the channel is working continously in multiplex mode	The path is available so the invalid CAW is a program error. Store a program check indication in the CSW, set the condition code to 01, and return to I-fetch	The multiplexor channel is in burst mode, or a circuit malfunction may be causing the problem. A time out signal will be issued to see if the channel is operational
Start I/O	If 1001: The start I/O was initiated on the Mpx ch, and a device end type interrupt may have to be reset. CC is set to 0, 2 or 3. If 0001: The start I/O was initiated on a Sel Ch. CC is set to 0, 2 or 3. Return to I-fetch	An immediate command has been executed, a malfunction has occurred, or the command was not accepted. The reason is indicated in the status of the CSW, the CC is set to 1, and the microprogram returns to I-fetch		not valid	

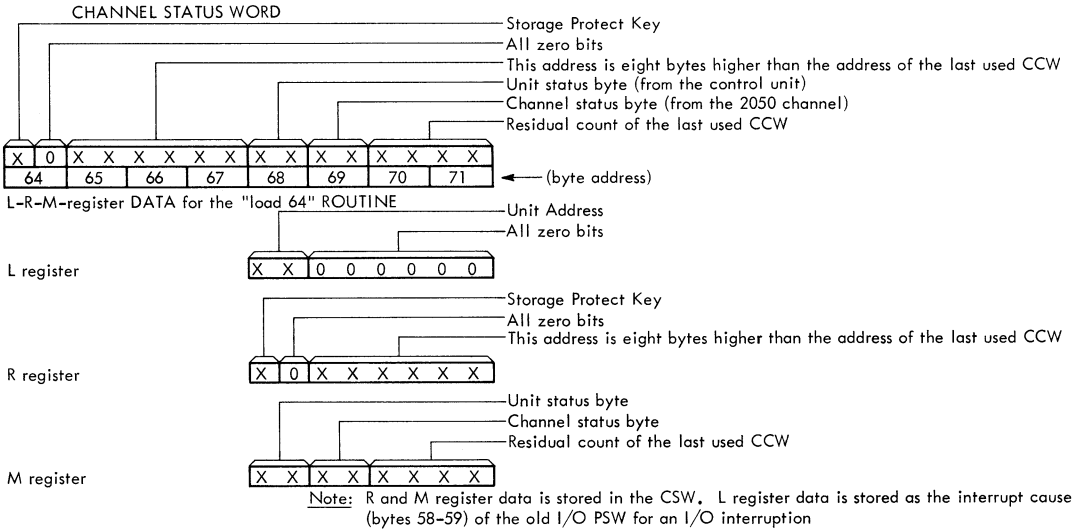
COMMON CHANNEL TO CPU REPLIES (SHEET 2 OF 3)

Request	X001	X011	X101	X111	Countdown/No Reply
Test I/O	The condition code has been set to 00, 10, or 11; return to I-fetch	Load the CSW from the data in the R and M register, set the condition code to 01, and return to I-fetch	The multiplexor channel requests a reset of the countdown. At the moment, the channel is working continuously in multiplex mode	not valid	The multiplexor channel is in burst mode, or a circuit malfunction may be causing the problem. A time out signal will be issued to see if the channel is operational
Halt I/O	The condition code has been set to 00, 10, or 11; return to I-fetch	A multiplex operation has been terminated. Load the unit and channel status into the CSW, set the condition code to 01, and return to I-fetch		not valid	
Proceed on Interrupt	Mpx reply: If it was a device end type, issue Interrupt Test I/O If it was any other type, fetch the interrupt data from 'bump', store it in the CSW, and Trap to the new I/O PSW	Sel reply: Load the CSW from the data in the R and M registers, and Trap to the new I/O PSW		not valid	

COMMON CHANNEL TO CPU REPLIES (SHEET 3 OF 3)

Request	X001	X011	X101	X111	Countdown/No Reply
Test Channel	The condition code has been set to 00, 01, 10, or 11; return to 1-fetch	not valid	not valid	not valid	Refer to Sheet 1 or 2
Interrupt Test I/O	not valid	Mpx reply: Load the CSW from the data in the R and M registers and Trap to the new I/O PSW	not valid	not valid	The multiplexor channel is in burst mode. Reset the IB full stat and return to 1-fetch
Time-out	The multiplexor channel is operating in burst mode, the condition code is set to 10 (2), and the microprogram returns to 1-fetch	not valid	not valid	not valid	Circuit Malfunction Either log the error or store "Ch Ctrl Ck" in the CSW and set the condition code to 01 (Eight cycle) countdown)
Time-out Check	This is the "die" signal to the channel, and no reply is expected				

Legend: X..not important 0..stat is off 1..stat is on


CHANNEL STATUS WORD
Storage Protect Key
All zero bits
This address is eight bytes higher than the address of the last used CCW
Unit status byte (from the control unit)
Channel status byte (from the 2050 channel)
Residual count of the last used CCW
X 0 X X X X X X X X X X X X X X
64 65 66 67 68 69 70 71
(byte address)
L-R-M-register DATA for the "load 64" ROUTINE
Unit Address
All zero bits
L register
X X 0 0 0 0 0 0
Storage Protect Key
All zero bits
This address is eight bytes higher than the address of the last used CCW
R register
X 0 X X X X X X
Unit status byte
Channel status byte
Residual count of the last used CCW
M register
X X X X X X X X
Note: R and M register data is stored in the CSW. L register data is stored as the interrupt cause (bytes 58-59) of the old I/O PSW for an I/O interruption

	Control or Data Error in CPU	Data Error in Channel	Control Error in Channel	Time Out	Time-Out Check
Normal Mode with PSW Bit 13=1	1. Error set into check reg 2. CPU and chan stop 3. CPU and chan are logged 4. Subchannel is reset 5. Machine check trap	Not applicable	1. Same as error in CPU	1. Mpx chan sets log request into CPU check reg 2. Same as error in CPU 3. If chan is unable to respond, then time out check will occur	1. Common chan sets log request into CPU check reg 2. Same as error in CPU
Normal Mode with PSW Bit 13=0	1. Error set into check reg 2. When PSW bit 13 goes to 1: a. CPU and chan stop b. CPU and chan are logged c. Currently operating subchannel is reset d. Machine check trap	Not applicable	1. Error is set into check reg 2. Operation on subchannel is terminated by sel reset 3. When PSW bit 13 goes to 1: a. CPU and chan are logged b. Currently operating subchannel is reset c. Machine check trap	1. Mpx chan sets log request into CPU check reg 2. Time out check will always occur	1. Common chan sets log request into CPU check reg 2. Set CC1 3. Load 64 with CCK 4. Operation on subchannel is terminated by sel reset 5. When bit 13 goes to 1: a. CPU and chan are logged b. Currently operating subchannel is reset c. Machine check trap
Stop Mode	1. Error set into check reg 2. CPU and chan stop	Not applicable	1. Same as error in CPU	1. Mpx sets log request into CPU check reg 2. Same as error in CPU . 3. If chan is unable to set check reg, then time out check	1. Common chan sets log request into CPU check reg 2. CPU and chan stop
Ignore Mode	1. Error set into check reg 2. No indication to chan 3. Operation continues	Not applicable	1. Error is set into check reg 2. Subchannel is reset 3. Machine check trap (no log out)	1. Ignore time-out signal	1. Common channel sets log request into CPU check reg 2. Set CC1 3. Load 64 with CK 4. Operation on subchannel is terminated by sel reset

	Control or Data Error in CPU	Data Error in Channel	Control Error in Channel	Time Out	Time-Out Check
Normal Mode with PSW Bit 13=1	1. Error set into CPU chk reg 2. Ctrl chk sent to ext chan 3. Chan stops 4. CPU and chan in error logged 5. Chan reset 6. Mach chk trap	1. Chan stops at end of record with data chk in its status reg 2. When chan not masked, as interrupt occurs	1. Chan stops with chan ctrl chk or IF ctrl chk in its status reg 2. When chan not masked, a chan log out occurs 3. After log out, an interrupt is forced 4. Chan is reset	1. Upon receipt of time out, chks for chan error conditions 2. If conditions exist, a chan log out is requested 3. After log out, CSW* is stored with chan ctrl chk or IF ctrl chk in chan status 4. Cond code set to 01 and chan reset 5. If error conditions not existing, time out chk occurs	1. Log request set into CPU chk reg Same as ctrl or data error in CPU
Normal Mode with PSW Bit 13=0	1. Error set into CPU chk reg 2. Log chan X latch in com chan set 3. No error signal sent to ext chan WHEN PSW BIT 13 = 1: 4. CPU and chan X are logged 5. Chan reset 6. Mach chk trap	Same as above	Same as above	Same as above	1. Log request set into CPU chk reg and chan stops with ctrl chk in status reg 2. Log chan X latch set 3. CSW* is stored and cond code set to 01 4. Chan is reset WHEN PSW BIT 13 = 1: 5. CPU and chan X logged 6. Chan is reset 7. Mach chk trap
Stop Mode or Chan Stop Mode	1. Error is displayed in CPU chk reg 2. Ctrl chk sent to chan 3. CPU and chan stopped	1. Channel stops 2. During initial selection, a log reg stops the CPU 3. After initial sel, if chan is not masked, a log req stops CPU	1. Channel stops 2. During initial selection, a log req stops the CPU 3. After initial sel, if chan is not masked, a log req stops the CPU	1. Channel stops 2. During initial selection, a log req stops CPU 3. After initial sel, if chan is not masked, a log req stops CPU	1. Same as ctrl or data error in CPU
Ignore Mode	1. Error is set into CPU chk reg 2. No error signal sent to ext chan	1. Chan stops at end of record with a data chk in its status reg 2. When chan not masked, an interrupt is requested (Same as normal mode with PSW bit 13 = 1)	1. Chan stops with chan ctrl chk or IF ctrl chk in its status reg 2. When chan not masked, an interrupt is requested (Same as normal mode with PSW bit 13 = 1, except no log out)	1. Ignore time out signal	1. Log request set into CPU chk reg 2. CSW* is stored with status chan ctrl chk 3. Cond code set to 01 4. Chan is reset

*Could be partial or complete CSW depending on op code.

Chan Read -- Data errors detected at the interface are corrected (parity inverted).

Chan Write -- Data errors detected at the interface are not corrected.

Chan Stop mode differs from stop mode in that the channel will stop on program, protect, and chain checks detected in channel in addition to above errors when in chan stop mode.

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